FUJITSU SEMICONDUCTOR
DATA SHEET

DS05-10163-2E

MEMORY

COS 4 M × 1 BIT FAST PAGE MODE DYNAMIC RAM

MB814100D-60/-70

CMOS 4,194,304 × 1 Bit Fast Mode Dynamic RAM

■ DESCRIPTION

The Fujitsu MB814100D is a fully decoded CMOS Dynamic RAM (DRAM) that contains 4,194,304 memory cells in 4M × 1 configuration. The MB814100D features a “fast page” mode of operation whereby high-speed random access of up to 2,048-bits of data within the same row can be selected. The MB814100D DRAM is ideally suited for mainframe, buffers, hand-held computers video imaging equipment, and other memory applications where very low power dissipation and wide bandwidth are basic requirements of the design. Since the standby current of the MB814100D is very small, the device can be used as a non-volatile memory in equipment that uses batteries for primary and/or auxiliary power.

The MB814100D is fabricated using silicon gate CMOS and Fujitsu’s advanced four-layer polysilicon process. This process, coupled with three-dimensional stacked capacitor memory cells, reduces the possibility of soft errors and extends the time interval between memory refreshes. Clock timing requirements for the MB814100D are not critical and all inputs are TTL compatible.

■ PRODUCT LINE & FEATURES

Parameter		MB814100D-60	MB814100D-70
$\overline{RAS}$ Access Time		60 ns max.	70 ns max.
$\overline{CAS}$ Access Time		15 ns max.	20 ns max.
Address Access Time		30 ns max.	35 ns max.
Randam Cycle Time		110 ns min.	125 ns min.
Fast Page Mode Cycle Time		40 ns min.	45 ns min.
Low Power Dissipation	Operating Current	605 mW max.	550 mW max.
	Standby Current	11 mW max. (TTL level) / 5.5 mW max. (CMOS level)	

- 4,194,304 words × 1 Bit organization
- Silicon gate, CMOS, 3D-Stacked capacitor Cell
- All input and output are TTL compatible
- 1024 refresh cycles every 16.4 ms
- $\overline{RAS}$ only, $\overline{CAS}$-before-$\overline{RAS}$, or Hidden Refresh
- Fast page Mode, Read-Modify-Write capability
- On chip substrate bias generator for high performance

This device contains circuitry to protect the inputs against damage due to high static voltages or electric fields. However, it is advised that normal precautions be taken to avoid application of any voltage higher than maximum rated voltages to this high impedance circuit.

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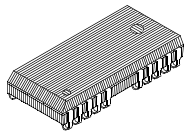
■ ABSOLUTE MAXIMUM RATINGS (See WARNING)

Parameter	Symbol	Value	Unit
Voltage at any pin relative to V_{SS}	V_{IN}, V_{OUT}	–1 to +7	V
Voltage of V_{CC} supply relative to V_{SS}	V_{CC}	–1 to +7	V
Power Dissipation	P_D	1.0	W
Short Circuit Output Current	I_{OUT}	±50	mA
Storage Temperature	T_{STG}	–55 to +125	°C

WARNING: Permanent device damage may occur if the above **Absolute Maximum Ratings** are exceeded. Functional operation should be restricted to the conditions as detailed in the operational sections of this data sheet. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

■ PACKAGE

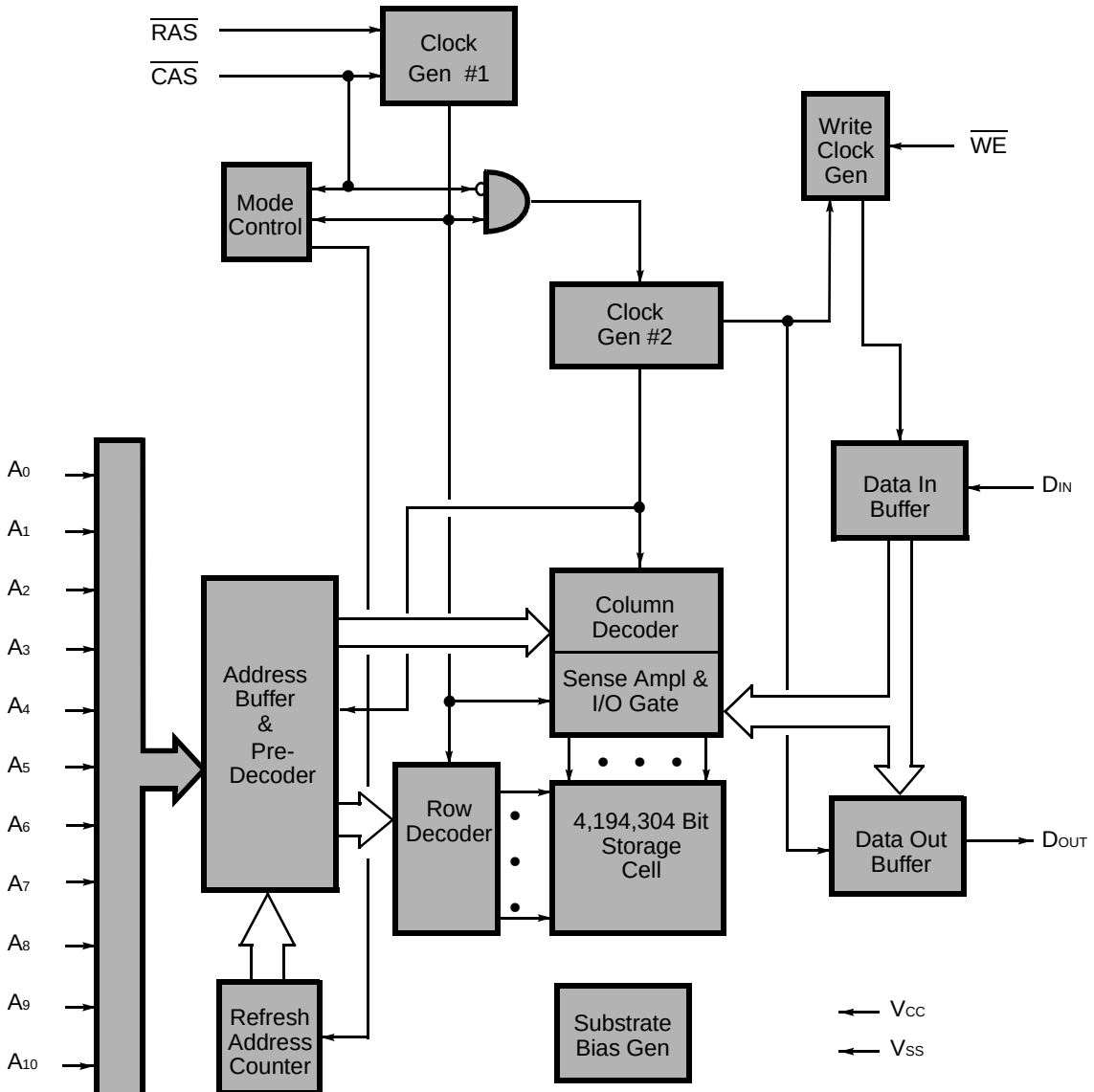


Plastic SOJ Package
(LCC-26P-M04)

Package and Ordering Information

– 26-pin plastic (300 mil) SOJ, order as MB814100D-xxPJN

Fig. 1 – MB814100D DYNAMIC RAM – BLOCK DIAGRAM



■ CAPACITANCE

(T_A=25°C, f = 1MHz)

Parameter	Symbol	Typ.	Max.	Unit
Input Capacitance, A_0 to A_{10}, D_{IN}	CIN_1	—	5	pF
Input Capacitance, $\overline{RAS}$, $\overline{CAS}$, $\overline{WE}$	CIN_2	—	7	pF
Output Capacitance, D_{OUT}	C_{OUT}	—	7	pF

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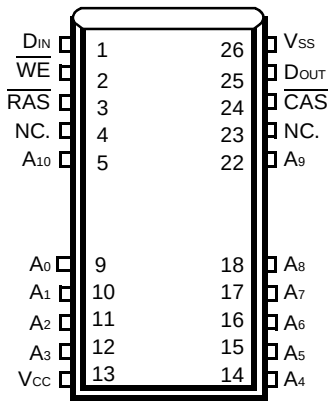
■ PIN ASSIGNMENTS AND DESCRIPTIONS

26-Pin SOJ:

(Top View)



Designator	Function
$\overline{WE}$	Write Enable.
$\overline{RAS}$	Row address strobe.
A_0 to A_{10}	Address inputs.
V_{CC}	+5 volt power supply.
$\overline{CAS}$	Column address strobe.
V_{SS}	Circuit ground.
D_{IN}	Data input
D_{OUT}	Data output

■ RECOMMENDED OPERATING CONDITIONS

Parameter	Notes	Symbol	Min.	Typ.	Max.	Unit	Ambient Operating Temp
Supply Voltage*	1	V_{CC}	4.5	5.0	5.5	V	0 5°C to + 70°C
		V_{SS}	0	0	0		
Input High Voltage, all inputs*	1	V_{IH}	2.4	—	6.5	V	
Input Low Voltage, all inputs*	1	V_{IL}	–2.0	—	0.8	V	

* : Reference Voltage : V_{SS} = 0 V

Note: Recommended operating conditions are the recommended values for guarantee of LSI's normal logic operations.
Under this conditions, the limits value of electrical characteristic (AD/DC)is guaranteed.

■ FUNCTIONAL OPERATION

ADDRESS INPUTS

Twenty two input bits are required to decode any one of 4,194,304 cell addresses in the memory matrix. Since only eleven address bits are available, the column and row inputs are separately strobed by CAS and RAS as shown in Figure 5. First, eleven row address bits are input on pins A_0-through-A_{10} and latched with the row address strobe (RAS) then, eleven column address bits are input and latched with the column address strobe (CAS). Both row and column addresses must be stable on or before the falling edge of CAS and RAS, respectively. The address latches are of the flow-through type; thus, address information appearing after t_{RAH} (min.)+ t_T is automatically treated as the column address.

WRITE ENABLE

The read or write mode is determined by the logic state of $\overline{WE}$. When $\overline{WE}$ is active Low, a write cycle is initiated; when $\overline{WE}$ is High, a read cycle is selected. During the read mode, input data is ignored.

DATA INPUT

Input data is written into memory in either of two basic ways--an early write cycle and a read-modify-write cycle. The falling edge of $\overline{WE}$ or CAS, whichever is later, serves as the input data-latch strobe. In an early write cycle, the input data is strobed by CAS and the setup/hold times are referenced to CAS because $\overline{WE}$ goes Low before CAS. In a delayed write or a read-modify-write cycle, $\overline{WE}$ goes Low after CAS; thus, input data is strobed by $\overline{WE}$ and all setup/hold times are referenced to the write-enable signal.

DATA OUTPUT

The three-state buffers are TTL compatible with a fanout of two TTL loads. Polarity of the output data is identical to that of the input; the output buffers remain in the high-impedance state until the column address strobe goes Low. When a read or read-modify-write cycle is executed, valid outputs are obtained under the following conditions:

t_{RAC} : from the falling edge of $\overline{RAS}$ when t_{RCD} (max.) is satisfied.
t_{CAC} : from the falling edge of CAS when t_{RCD} is greater than t_{RCD} (max.).
t_{AA} : from column address input when t_{RAD} is greater than t_{RAD} (max.).

The data remains valid until $\overline{CAS}$ returns to a High logic level. When an early write is executed, the output buffers remain in a high-impedance state during the entire cycle.

FAST PAGE MODE OF OPERATION

The fast page mode of operation provides faster memory access and lower power dissipation. The fast page mode is implemented by keeping the same row address and strobing in successive column addresses. To satisfy these conditions, $\overline{RAS}$ is held Low for all contiguous memory cycles in which row addresses are common. For each fast page of memory, any of 2,048-bits can be accessed and, when multiple MB 814100Ds are used, CAS is decoded to select the desired memory fast page. Fast page mode operations need not be addressed sequentially and combinations of read, write, and/or read-modify-write cycles are permitted.

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■ DC CHARACTERISTICS

(Recommended operating conditions unless otherwise noted.) Note 3

Parameter		Notes	Symbol	Condition	Values			Unit
					Min.	Typ.	Max.	
Output High Voltage		1	V_{OH}	I_{OH} = –5.0 mA	2.4	—	—	V
Output Low Voltage		1	V_{OL}	I_{OL} = 4.2 mA	—	—	0.4	
Input Leakage Current (Any Input)			$I_{I(L)}$	0 V ≤ V_{IN} 5.5 V; 4.5 V ≤ V_{CC} ≤ 5.5 V; V_{SS} = 0 V; All other pins not under test = 0 V	–10	—	10	µA
Output Leakage Current			$I_{O(L)}$	0V≤V_{OUT}≤5.5V; Data out disabled	–10	—	10	
Operating Current (Average Power Supply Current)	MB814100D-60	2	I_{CC1}	$\overline{RAS}$ & $\overline{CAS}$ cycling; t_{RC} = min.	—	—	110	mA
	MB814100D-70						100	
Standby Current (Power Supply Current)	TTL level		I_{CC2}	$\overline{RAS}$ = $\overline{CAS}$ = V_{IH}	—	—	2.0	mA
	CMOS level			$\overline{RAS}$ = $\overline{CAS}$ ≥ V_{CC} – 0.2 V			1.0	
Refresh Current #1 (Average Power Supply Current)	MB814100D-60	2	I_{CC3}	$\overline{CAS}$ = V_{IH}, $\overline{RAS}$ cycling; t_{RC} = min.	—	—	110	mA
	MB814100D-70						100	
Fast Page Mode Current	MB814100D-60	2	I_{CC4}	$\overline{RAS}$ = V_{IL}, $\overline{CAS}$ cycling; t_{PC} = min.	—	—	55	mA
	MB814100D-70						50	
Refresh Current #2 (Average Power Supply Current)	MB814100D-60	2	I_{CC5}	$\overline{RAS}$ cycling; $\overline{CAS}$-before-$\overline{RAS}$; t_{RC} = min.	—	—	110	mA
	MB814100D-70						100	

■ AC CHARACTERISTICS

(At recommended operating conditions unless otherwise noted.) Notes 3, 4, 5

No.	Parameter	Notes	Symbol	MB814100D-60		MB814100D-70		Unit
				Min.	Max.	Min.	Max.	
1	Time Between Refresh		t_{REF}	—	16.4	—	16.4	ms
2	Random Read/Write Cycle Time		t_{RC}	110	—	125	—	ns
3	Read-Modify-WriteCycle Time		t_{RWC}	130	—	150	—	ns
4	Access Time from $\overline{RAS}$		t_{RAC}	—	60	—	70	ns
5	Access Time from $\overline{CAS}$	6, 9	t_{CAC}	—	15	—	20	ns
6	Column Address Access Time	7, 9	t_{AA}	—	30	—	35	ns
7	Output Hold Time	8, 9	t_{OH}	0	—	0	—	ns
8	Output Buffer Turn On Delay Time		t_{ON}	0	—	0	—	ns
9	Output Buffer Turn Off Delay Time	10	t_{OFF}	—	15	—	15	ns
10	Transition Time		t_T	2	50	2	50	ns
11	$\overline{RAS}$ Precharge Time		t_{RP}	40	—	45	—	ns
12	$\overline{RAS}$ Pulse Width		t_{RAS}	60	100000	70	100000	ns
13	$\overline{RAS}$ Hold Time		t_{RSH}	15	—	20	—	ns
14	$\overline{CAS}$ to RAS Precharge Time		t_{CRP}	5	—	5	—	ns
15	$\overline{RAS}$ to CAS Delay Time	11, 12	t_{RCD}	20	45	20	50	ns
16	$\overline{CAS}$ Pulse Width		t_{CAS}	15	—	20	—	ns
17	$\overline{CAS}$ Hold Time		t_{CSH}	60	—	70	—	ns
18	$\overline{CAS}$ Precharge Time (Normal)	17	t_{CPN}	10	—	10	—	ns
19	Row Address Set Up Time		t_{ASR}	0	—	0	—	ns
20	Row Address Hold Time		t_{RAH}	10	—	10	—	ns
21	Column Address Set Up Time		t_{ASC}	0	—	0	—	ns
22	Column Address Hold Time		t_{CAH}	15	—	15	—	ns
23	$\overline{RAS}$ to Column Address Delay Tim	13	t_{RAD}	15	30	15	35	ns
24	Column Address to $\overline{RAS}$ Lead Time		t_{RAL}	30	—	35	—	ns
25	Column Address to $\overline{CAS}$ Lead Time		t_{CAL}	30	—	35	—	ns
26	Read Command Set Up Time		t_{RCS}	0	—	0	—	ns
27	Read Command and Hold Time Referenced to $\overline{RAS}$	14	t_{RRH}	0	—	0	—	ns
28	Read Command and Hold Time Referenced to $\overline{CAS}$	14	t_{RCH}	0	—	0	—	ns
29	Write Command Set Up Time	15	t_{WCS}	0	—	0	—	ns
30	Write Command Hold Time		t_{WCH}	10	—	10	—	ns

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■ AC CHARACTERISTICS (Continued)

(At recommended operating conditions unless otherwise noted.) Notes 3, 4, 5

No.	Parameter	Notes	Symbol	MB814100D-60		MB814100D-70		Unit
				Min.	Max.	Min.	Max.	
31	$\overline{WE}$ Pulse Width		t_{WP}	10	—	10	—	ns
32	Write Command to $\overline{RAS}$ Lead Time		t_{RWL}	15	—	20	—	ns
33	Write Command to $\overline{CAS}$ Lead Time		t_{CWL}	20	—	20	—	ns
34	DIN Set Up Time		t_{DS}	0	—	0	—	ns
35	DIN Hold Time	19	t_{DH}	15/18	—	15/18	—	ns
36	$\overline{RAS}$ to $\overline{WE}$ Delay Time	15	t_{RWD}	60	—	70	—	ns
37	$\overline{CAS}$ to $\overline{WE}$ Delay Time	15	t_{CWD}	15	—	20	—	ns
38	Column Address to $\overline{WE}$ Lead Time	15	t_{AWD}	30	—	35	—	ns
39	$\overline{RAS}$ Precharge Time to $\overline{CAS}$ Active Time (Refresh cycles)		t_{RPC}	10	—	10	—	ns
40	$\overline{CAS}$ Set Up Time for $\overline{CAS}$ -before-$\overline{RAS}$ Refresh		t_{CSR}	0	—	0	—	ns
41	$\overline{CAS}$ Hold Time for $\overline{CAS}$ -before-$\overline{RAS}$ Refresh		t_{CHR}	10	—	10	—	ns
42	$\overline{WE}$ Set Up Time from $\overline{RAS}$*18	18	t_{WSR}	10	—	10	—	ns
43	$\overline{WE}$ Hold Time from $\overline{RAS}$*18	18	t_{WHR}	10	—	10	—	ns
44	Fast Page Mode $\overline{RAS}$ Pulse Width		t_{RASP}	—	200000	—	200000	ns
45	Fast Page Mode Read/Write Cycle Time		t_{PC}	40	—	45	—	ns
46	Fast Page Mode Read-Modify-Write Cycle Time		t_{PRWC}	65	—	70	—	ns
47	Access Time from $\overline{CAS}$ Precharge	9, 16	t_{CPA}	—	35	—	40	ns
48	Fast Page Mode $\overline{CAS}$ Precharge Time		t_{CP}	10	—	10	—	ns
49	Fast Page Mode $\overline{RAS}$ Hold Time $\overline{CAS}$ Precharge		t_{RHCP}	35	—	40	—	ns
50	Fast Page Mode $\overline{CAS}$ Precharge Time $\overline{WE}$ Delay Time		t_{CPWD}	35	—	40	—	ns

Notes:
1. Referenced to V_{SS}.
2. I_{CC} depends on the output load conditions and cycle rates; The specified values are obtained with the output open.
   I_{CC} depends on the number of address change as $\overline{RAS} = V_{IL}$ and $\overline{CAS} = V_{IH}$, $V_{IL} > -0.5$ V. I_{CC1}, I_{CC3} and I_{CC5} are specified at one time of address change during $\overline{RAS} = V_{IL}$ and $\overline{CAS} = V_{IH}$. I_{CC4} is specified at one time of address change during one Page cycle.
3. An Initial pause ($\overline{RAS}$=$\overline{CAS}$=V_{IH}) of 200 µs is required after power-up followed by $\overline{RAS}$ only refresh cycle or $\overline{CAS}$ before $\overline{RAS}$ refresh cycle (WE= "H") before proper device operation is achieved. In case of using internal refresh counter, a minimum of eight $\overline{CAS}$ -before-$\overline{RAS}$ initialization cycles instead of $\overline{RAS}$ only refresh cycle are required.
4. AC characteristics assume t_T = 5 ns.
5. V_{IH} (min.) and V_{IL} (max.) are reference levels for measuring timing of input signals. Also transition times are measured between V_{IH} (min.) and V_{IL} (max.).
6. Assumes that $t_{RCD} \leq t_{RCD}$ (max.) and $t_{RAD} \leq t_{RAD}$ (max.). If $t_{RCD} > t_{RCD}$ (max.) or $t_{RAD} > t_{RAD}$ (max.), t_{RAC} will be increased by the amount that t_{RCD} or t_{RCD} exceeds the maximum recommended value shown in this table. Refer to Fig. 2 and 3.
7. If $t_{RCD} \geq t_{RCD}$ (max.), $t_{RAD} \geq t_{RAD}$ (max.), and $t_{ASC} \geq t_{AA} - t_{CAC} - t_T$, access time is t_{CAC}.
8. If $t_{RAD} \geq t_{RAD}$ (max.) and $t_{ASC} \leq t_{AA} - t_{CAC} - t_T$, access time is t_{AA}.
9. Measured with a load equivalent to two TTL loads and 100 pF.
10. t_{OFF} is specified that output buffer change to high impedance state.
11. Operation within the t_{RCD} (max.) limit ensures that t_{RAC} (max.) can be met. t_{RCD} (max.) is specified as a reference point only; if t_{RCD} is greater than the specified t_{RCD} (max.) limit, access time is controlled exclusively by t_{CAC} or t_{AA}.
12. t_{RCD} (min.) = t_{RAH} (min.)+ 2 t_T + t_{ASC} (min.).
13. Operation within the t_{RAD} (max.) limit ensures that t_{RAC} (max.) can be met. t_{RAD} (max.) is specified as a reference point only; if t_{RAD} is greater than the specified t_{RAD} (max.) limit, access time is controlled exclusively by t_{CAC} or t_{AA}.
14. Either t_{RRH} or t_{RCH} must be satisfied for a read cycle.
15. t_{WCS}, t_{RWD}, t_{CWD} and t_{AWD} are not restrictive operating parameters. They are included in the data sheet as electrical characteristics only. If $t_{WCS} \geq t_{WCS}$ (min.), the cycle is a Early-Write cycle and data out pin will remain open circuit (high impedance) through the entire cycle. If $t_{WRD} \geq t_{WRD}$ (min.), $t_{CWD} \geq t_{CWD}$ (min.) and $t_{AWD} \geq t_{AWD}$ (min.), the cycle is a Read-Modify-Write cycle and data out pin will contain data read from the selected cell. If WE is falled when neither of above sets of conditions is satisfied, the cycle is a Delayed-Write cycle and the writing to the selected cell is executed when t_{RWL}, t_{CWL}, t_{CAL} and t_{RAL} are satisfied, but the condition of the data out pin is indeterminated.
16. t_{CPA} is access time from the selection of a new column address (that is caused by changing $\overline{CAS}$ from "L" to "H"). Therefore, if t_{CP} is long, t_{CPA} is longer than t_{CPA} (max.).
17. Assumes that $\overline{CAS}$-before-$\overline{RAS}$ refresh.
18. Assumes that Test mode function.
19. If $t_{RCD} \leq t_{RCD}$ (max.), t_{DH} = 18 ns. Otherwise, t_{DH} = 15 ns

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Fig. 2 – t_{RAC} vs. t_{RCD}

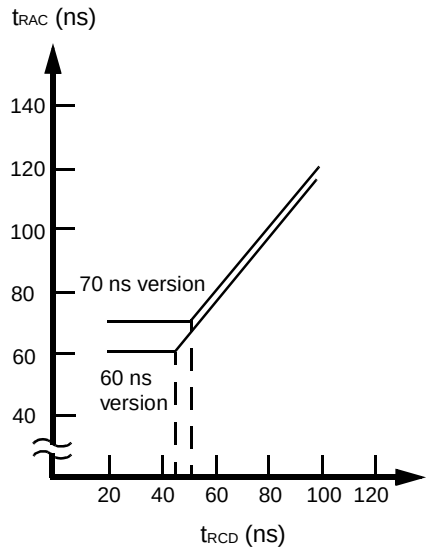


Fig. 3 – t_{RAC} vs. t_{RAD}

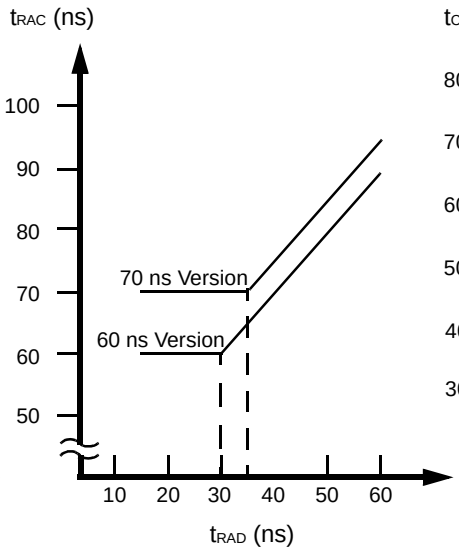
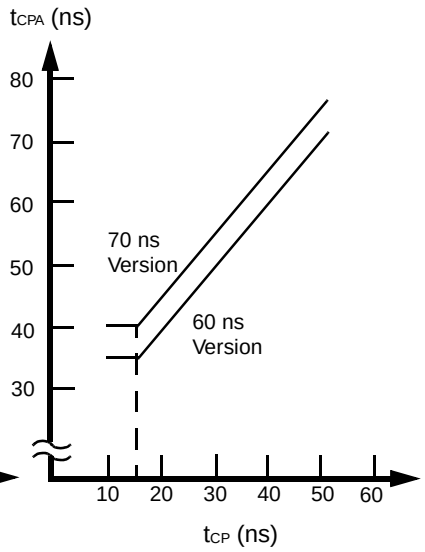


Fig. 4 – t_{CPA} vs. t_{CP}



■ FUNCTIONAL TRUTH TABLE

Operation Mode	Clock Input			Address		Input Data		Refresh	Note
	$\overline{RAS}$	$\overline{CAS}$	$\overline{WE}$	Row	Column	Input	Oupput		
Standby	H	H	X	—	—	—	High-Z	—	
Read Cycle	L	L	H	Valid	Valid	—	Valid	Yes*	$t_{RCS} \geq t_{RCS}$ (min.)
Write Cycle (Early Write)	L	L	L	Valid	Valid	Valid	High-Z	Yes*	$t_{WCS} \geq t_{WCS}$ (min.)
Read-Modify-Write Cycle	L	L	H→L	Valid	Valid	X→ Valid	Valid	Yes*	$t_{CWD} \geq t_{CWD}$ (min.)
$\overline{RAS}$-only Refresh Cycle	L	H	X	Valid	—	—	High-Z	Yes	
$\overline{CAS}$-before-$\overline{RAS}$ Refresh Cycle	L	L	H	—	—	—	High-Z	Yes	$t_{CSR} \geq t_{CSR}$ (min.)
Hidden Refresh Cycle	H→L	L	H	—	—	—	Valid	Yes	Previous data is kept.
Test Mode Set Cycle (CBR)	L	L	L	—	—	—	High-Z	Yes	$t_{CSR} \geq t_{CSR}$ (min.) $t_{WSR} \geq t_{WSR}$ (min.)
Test Mode Set Cycle (Hidden)	H→L	L	L	—	—	—	Valid	Yes	$t_{CSR} \geq t_{CSR}$ (min.) $t_{WSR} \geq t_{WSR}$ (min.)

X; “H” or “L”
*; It is impossible in Fast Page Mode

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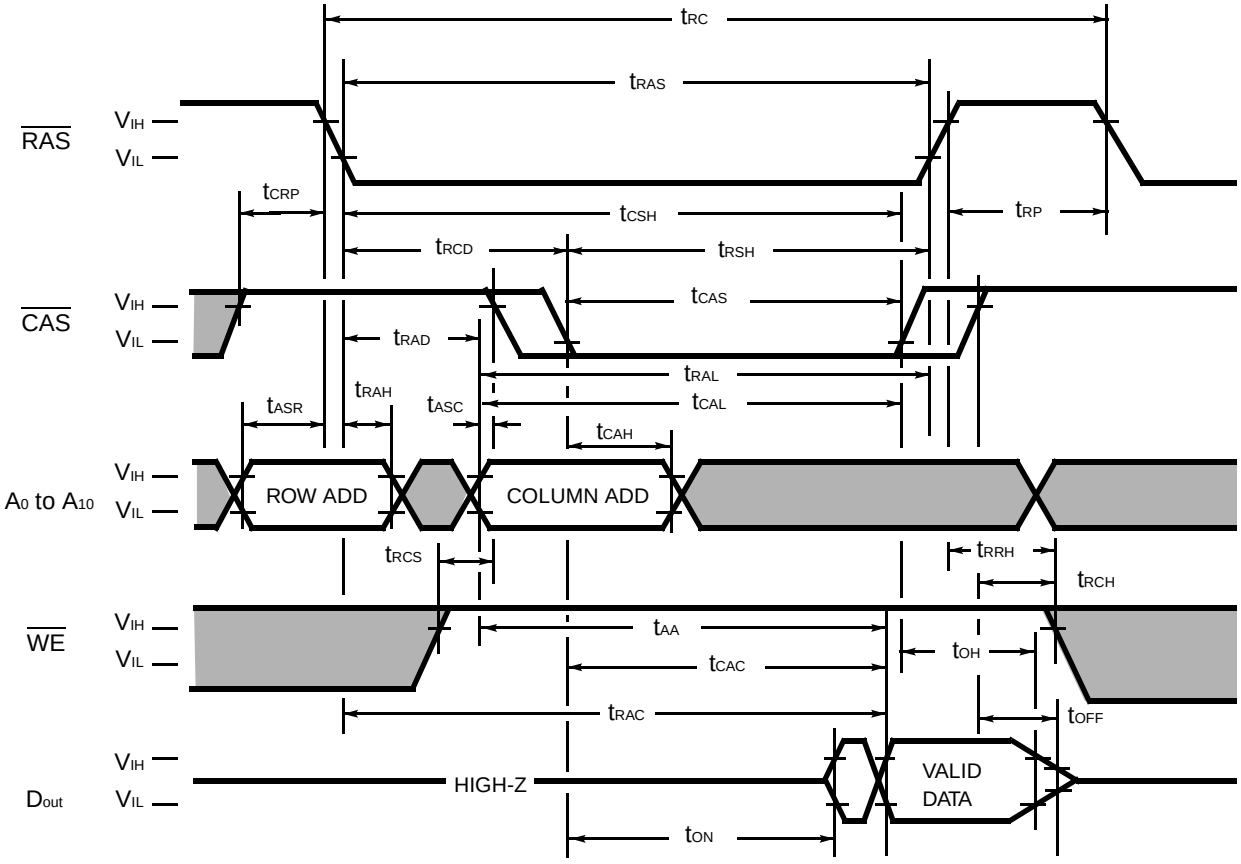
Fig. 5 – READ CYCLE

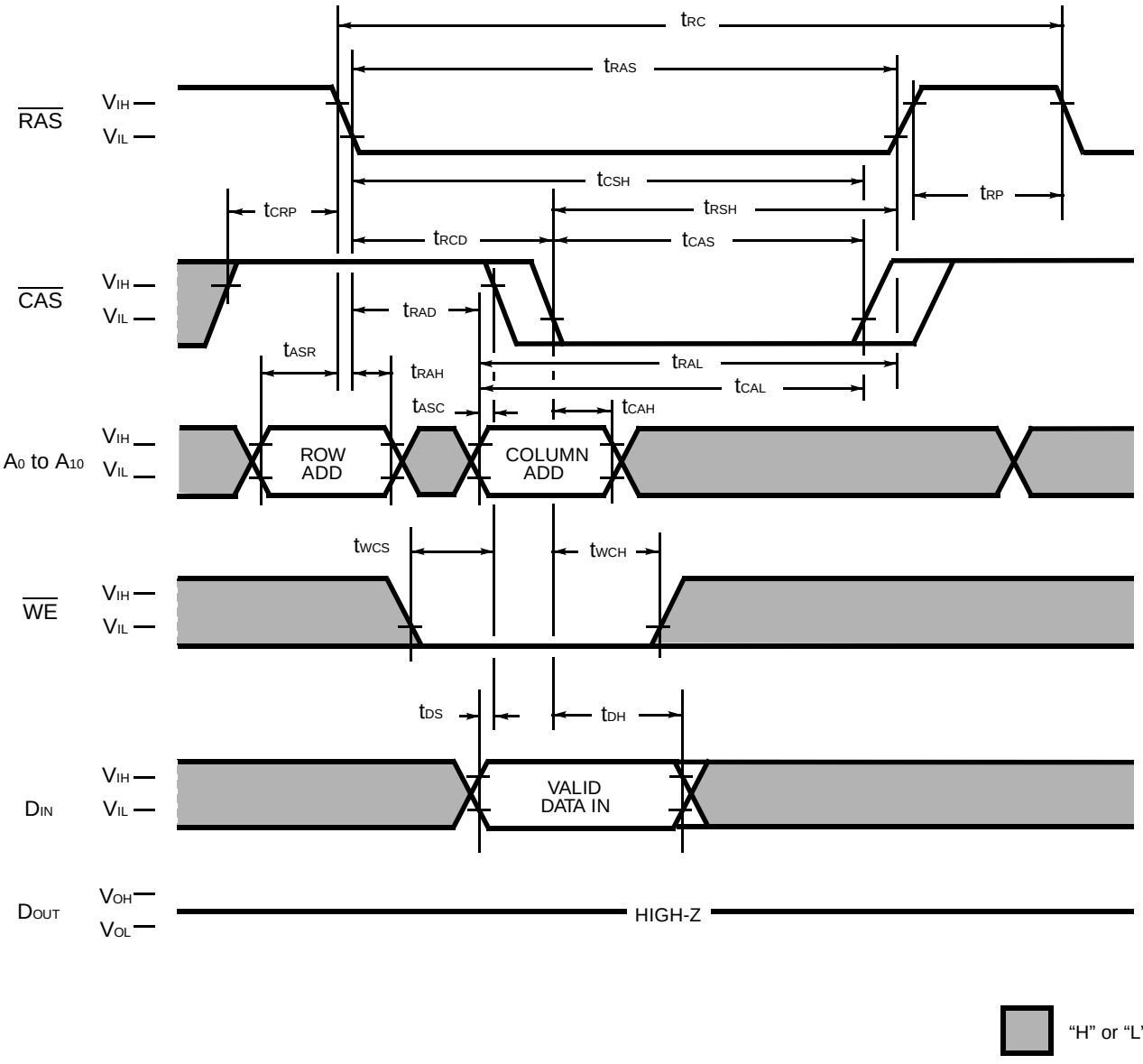


DESCRIPTION

To implement a read operation, a valid address is latched in by the $\overline{RAS}$ and $\overline{CAS}$ address strobes and with $\overline{WE}$ set to a High level, the output is valid once the memory access time has elapsed. The access time is determined by RAS(t_{RAC}), CAS(t_{CAC}), or column addresses (t_{AA}), if t_{RCD} ($\overline{RAS}$ to $\overline{CAS}$ delay time) is greater than the specification, the access time is t_{AA} under the following conditions:

If $t_{RCD} > t_{RCD}$ (max.), access time = t_{CAC}.
If $t_{RAD} > t_{RAD}$ (max.), access time = t_{AA}.

Fig. 6 – EARLY WRITE CYCLE



DESCRIPTION

A write cycle is similar to a read cycle except $\overline{WE}$ is set to a Low state. A write cycle can be implemented in either of two ways - early write or read-modify-write. The input data is latched with the later falling edge of $\overline{CAS}$ or $\overline{WE}$ and written into memory. During all write cycles, timing parameters t_{RWL}, t_{CWL}, t_{CAL} and t_{RAL} must be satisfied.

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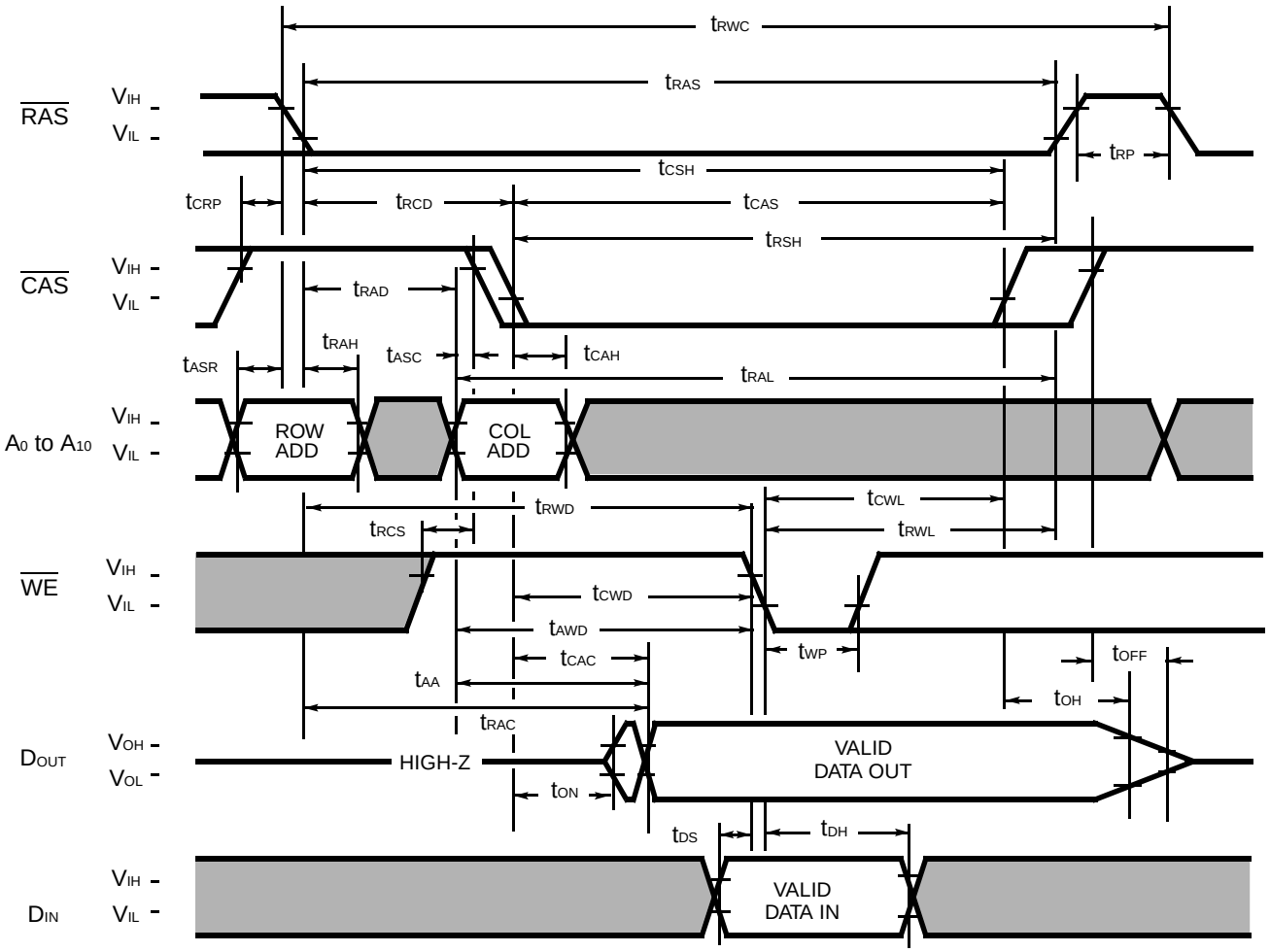
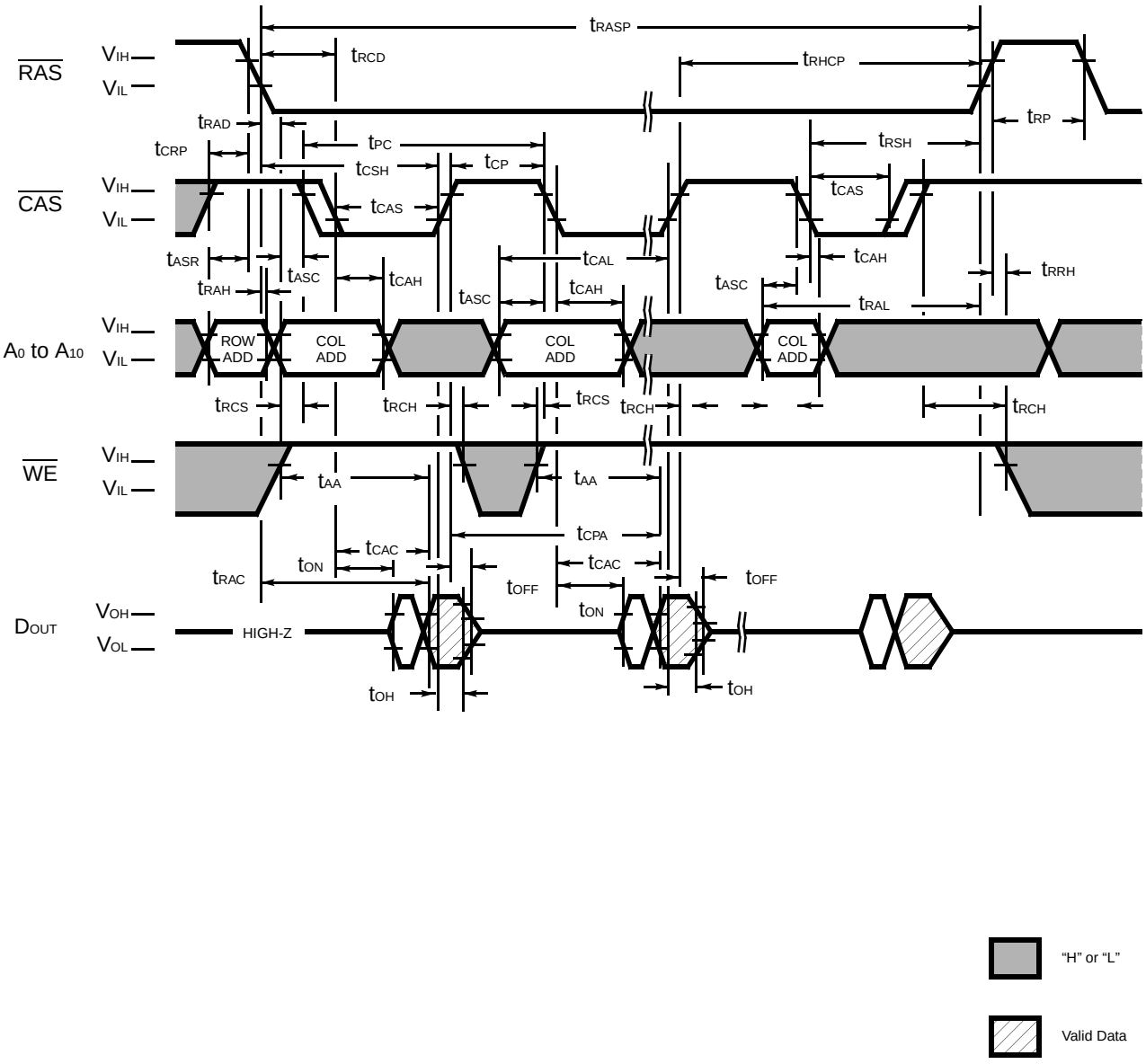
Fig. 7 – READ–MODIFY–WRITE–CYCLE



DESCRIPTION

The read-modify-write cycle is executed by changing $\overline{WE}$ from High to Low after the read operation is implemented.

Fig. 8 – FAST PAGE MODE READ CYCLE



DESCRIPTION

The fast page mode read cycle is executed after normal cycle with holding $\overline{RAS}$ "L", applying column address and $\overline{CAS}$, and keeping $\overline{WE}$ "H" . Once an address is selected normally using the $\overline{RAS}$ and $\overline{CAS}$, other addresses in the same row can be selected by only changing the column address and applying the $\overline{CAS}$.
Any of the 2048 bits belonging to each row can be accessed.

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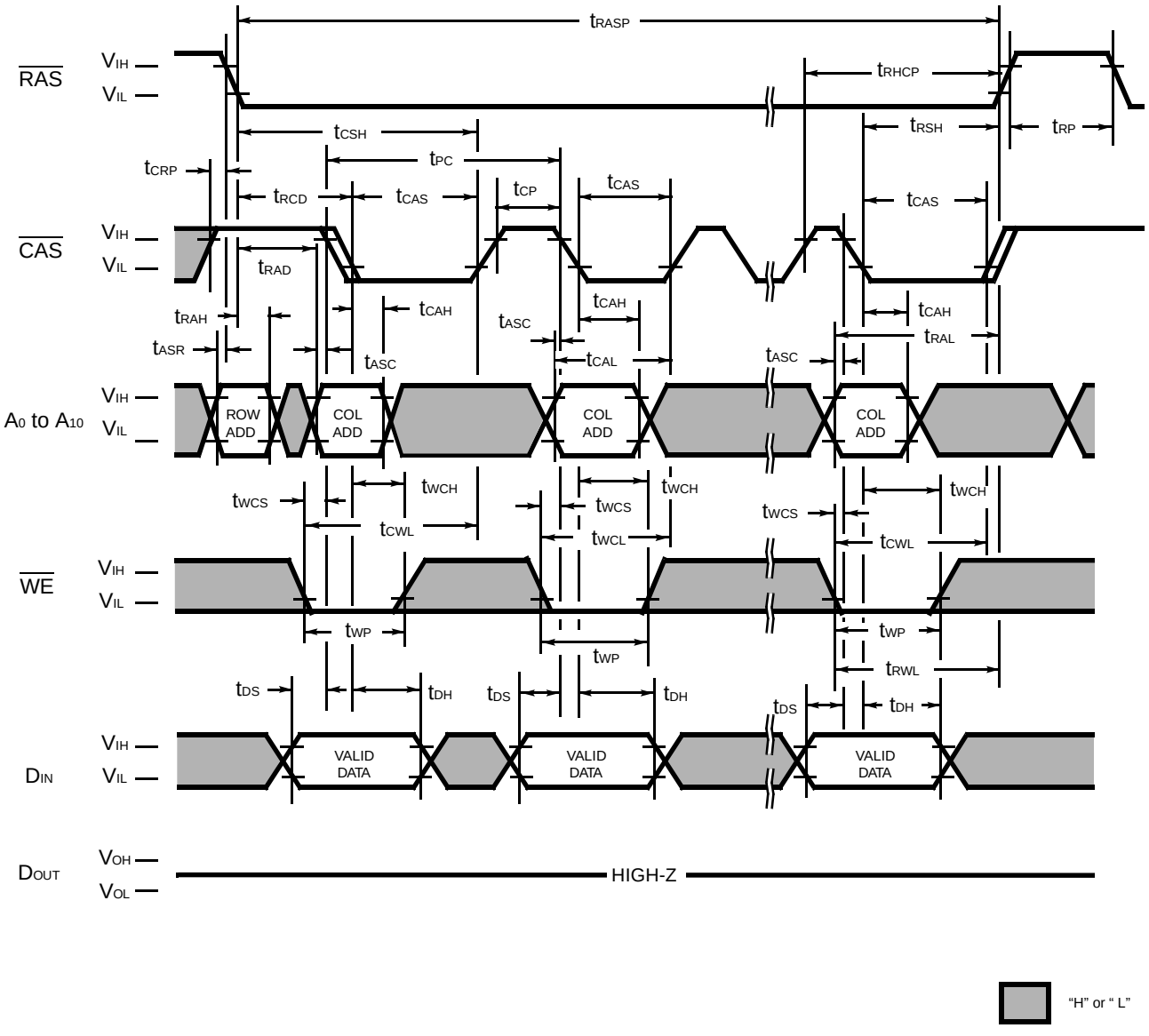
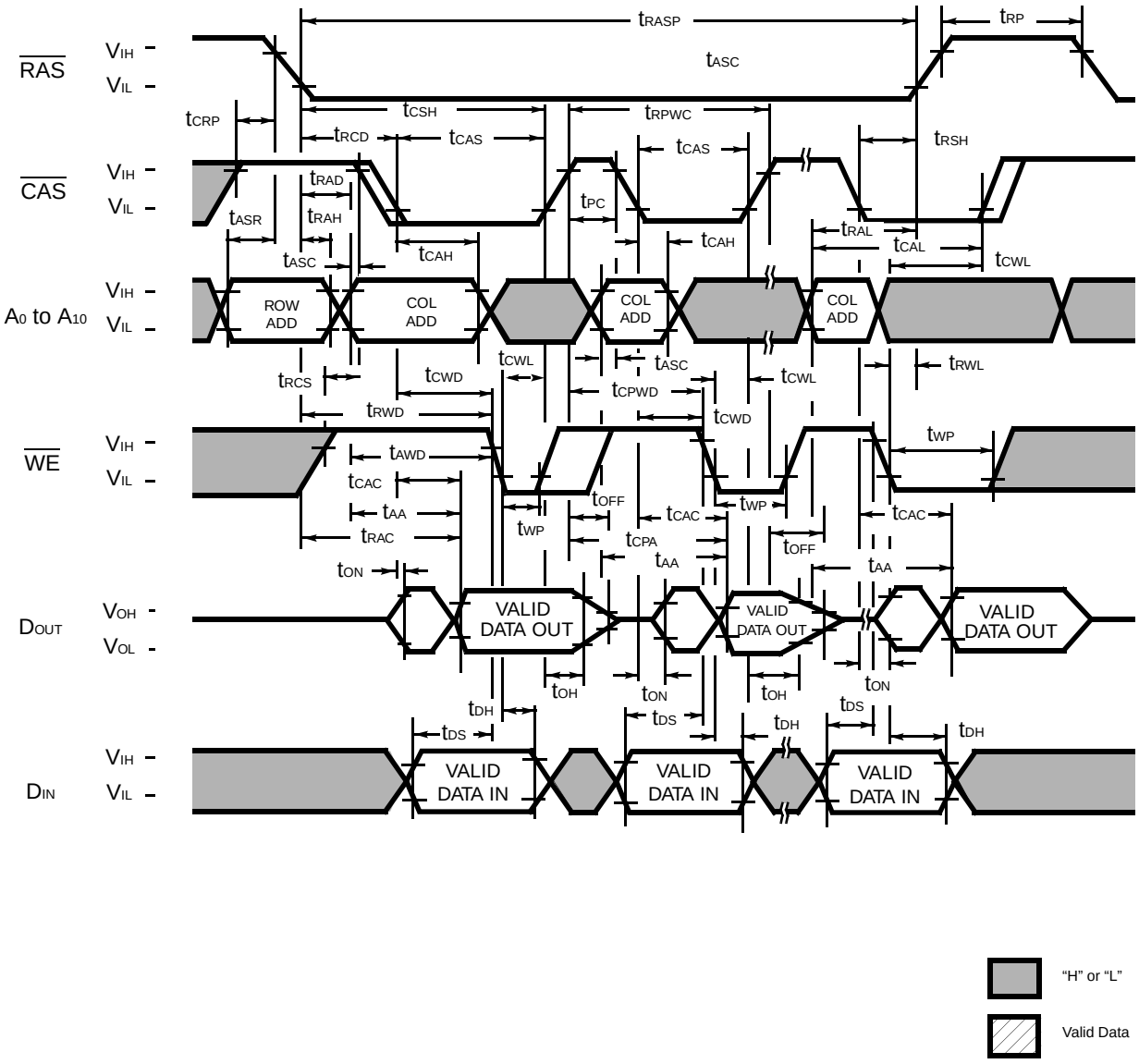
Fig. 9 – FAST PAGE MODE WRITE CYCLE (EARLY WRITE CYCLE)



DESCRIPTION

The fast page mode write cycle is executed by the same manner as fast page mode read cycle except for the state of $\overline{WE}$
The data on DIN pin is latched with the falling edge of $\overline{CAS}$ and written into the memory. The input data is latched with the later falling edge of $\overline{CAS}$ or $\overline{WE}$ and written into memory. Any of the 2048 bits belonging to each row can be accessed.
In this mode, refresh operation is not supported . The condition of refresh time must be satisfied and $\overline{RAS}$ timing must be determined well.

Fig. 10 – FAST PAGE MODE READ-MODIFY–WRITE CYCLE



DESCRIPTION

During fast page mode, the read-modify-write cycle can be executed by changing $\overline{WE}$ high to low after the data appears at D pin as well as normal cycle.

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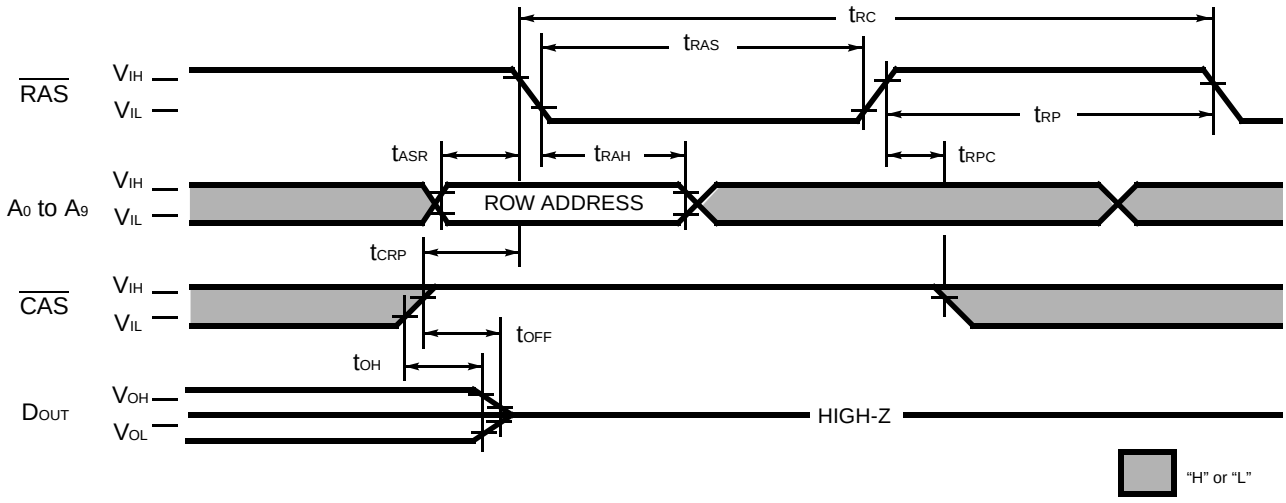
Fig. 11 – $\overline{RAS}$–ONLY REFRESH ($\overline{WE}$ = A_{IO} = ”H” or ”L”)

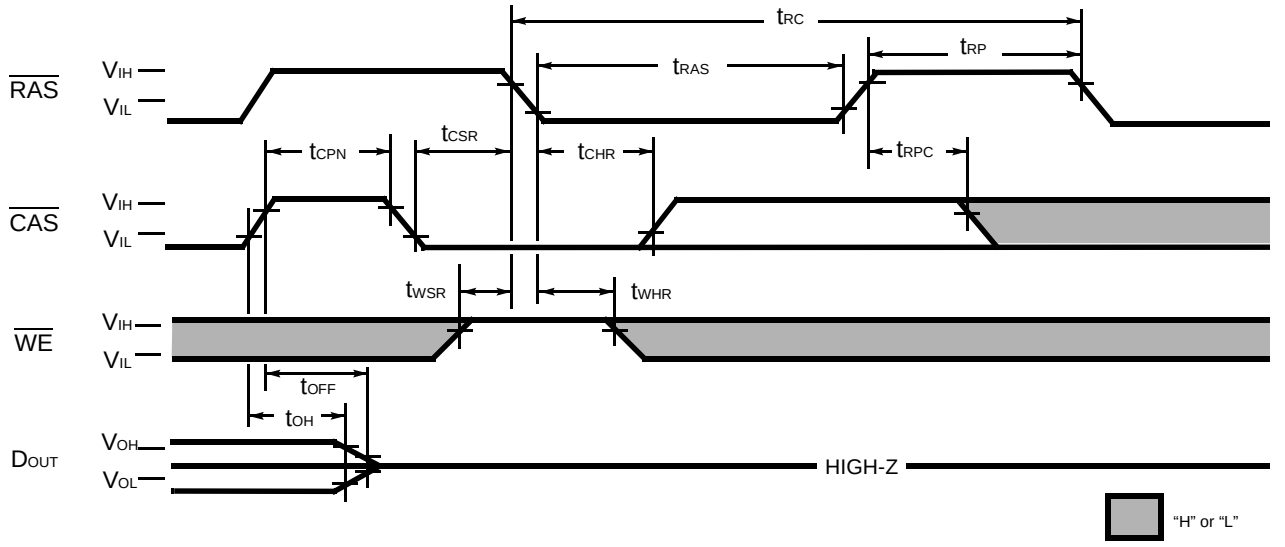


DESCRIPTION

Refresh of DRAM memory cells is accomplished by performing a read, a write, or a read-modify-write cycle at each of 1024 row addresses every 16.4-milliseconds.

$\overline{RAS}$-only refresh is performed by keeping $\overline{CAS}$ High throughout the cycle; D pin is kept in a high-impedance state.

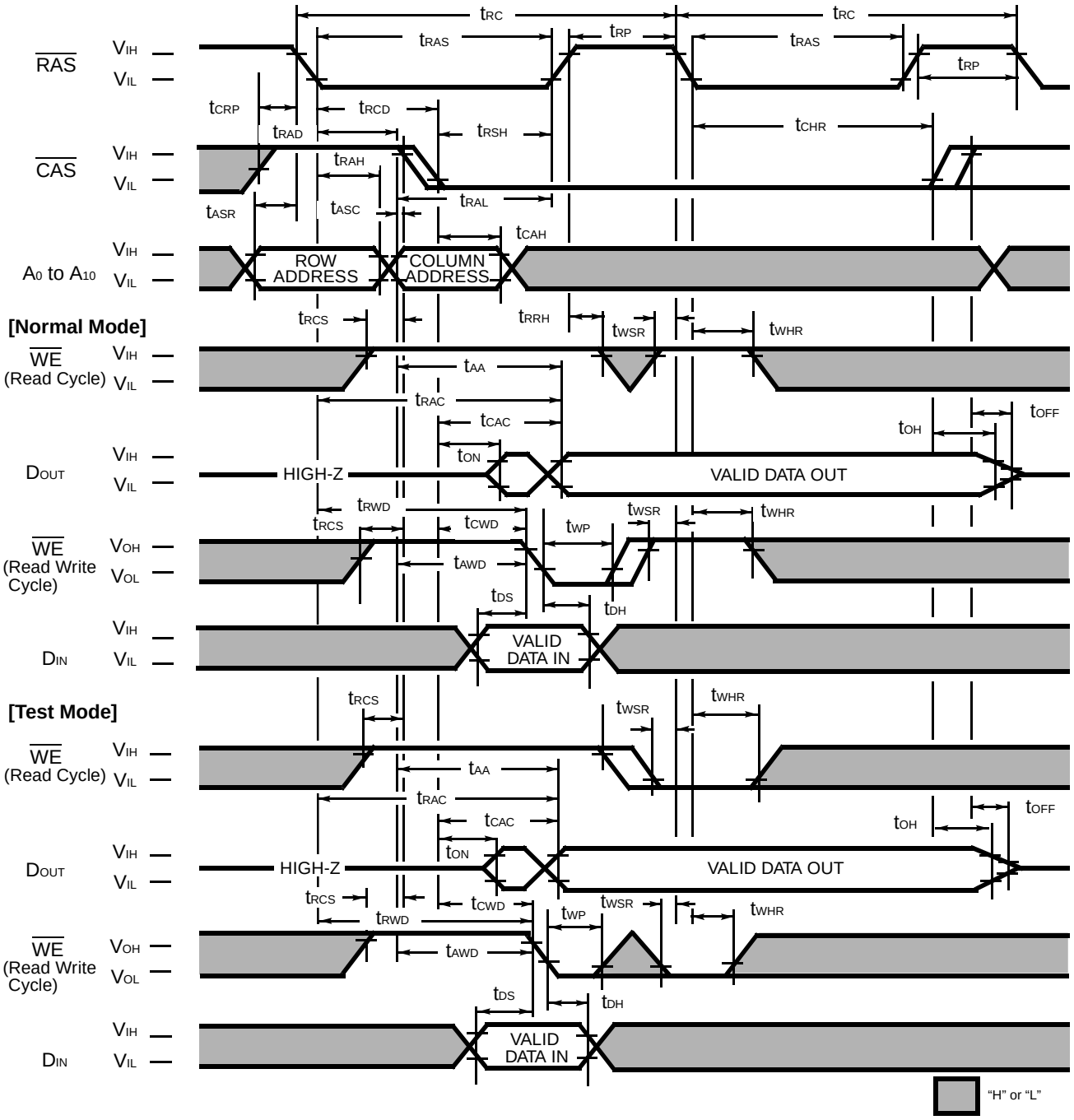
Fig. 12 – $\overline{CAS}$-BEFORE–$\overline{RAS}$ REFRESH (ADDRESS = D_{IN} = ”H” or ”L”)



DESCRIPTION

$\overline{CAS}$-before-$\overline{RAS}$ refresh is an on-chip refresh capability that eliminates the need for external refresh addresses. If $\overline{CAS}$ is held Low for the specified setup time (t_{CSR}) before $\overline{RAS}$ goes Low, the on-chip refresh control clock generators and refresh address counter are enabled. An internal refresh operation automatically occurs and the refresh address counter is internally incremented in preparation for the next $\overline{CAS}$-before-$\overline{RAS}$ refresh operation.
$\overline{WE}$ must be held High for the specified set up time (t_{WSR}) before $\overline{RAS}$ goes low in order not to enter ”test mode”.

Fig. 13 – HIDDEN REFRESH CYCLE



DESCRIPTION

The hidden refresh is executed by keeping $\overline{CAS}$ "L" to next cycle, i.e., the output data at previous cycle is kept during next refresh cycle. Since the $\overline{CAS}$ is kept low continuously from previous cycle, followed refresh cycle should be $\overline{CAS}$-before-$\overline{RAS}$ refresh.
$\overline{WE}$ must be held "H" for the specified set up time (t_{WSR}) before $\overline{RAS}$ goes "L" for the second time in order not to enter "test mode" to be specified later.
In addition, when a hidden refresh is executed, $\overline{CAS}$ must be high by the specified timing t_{CRP} before read cycle, write cycle, read-write/ read-modify-write or page-mode cycle is executed.

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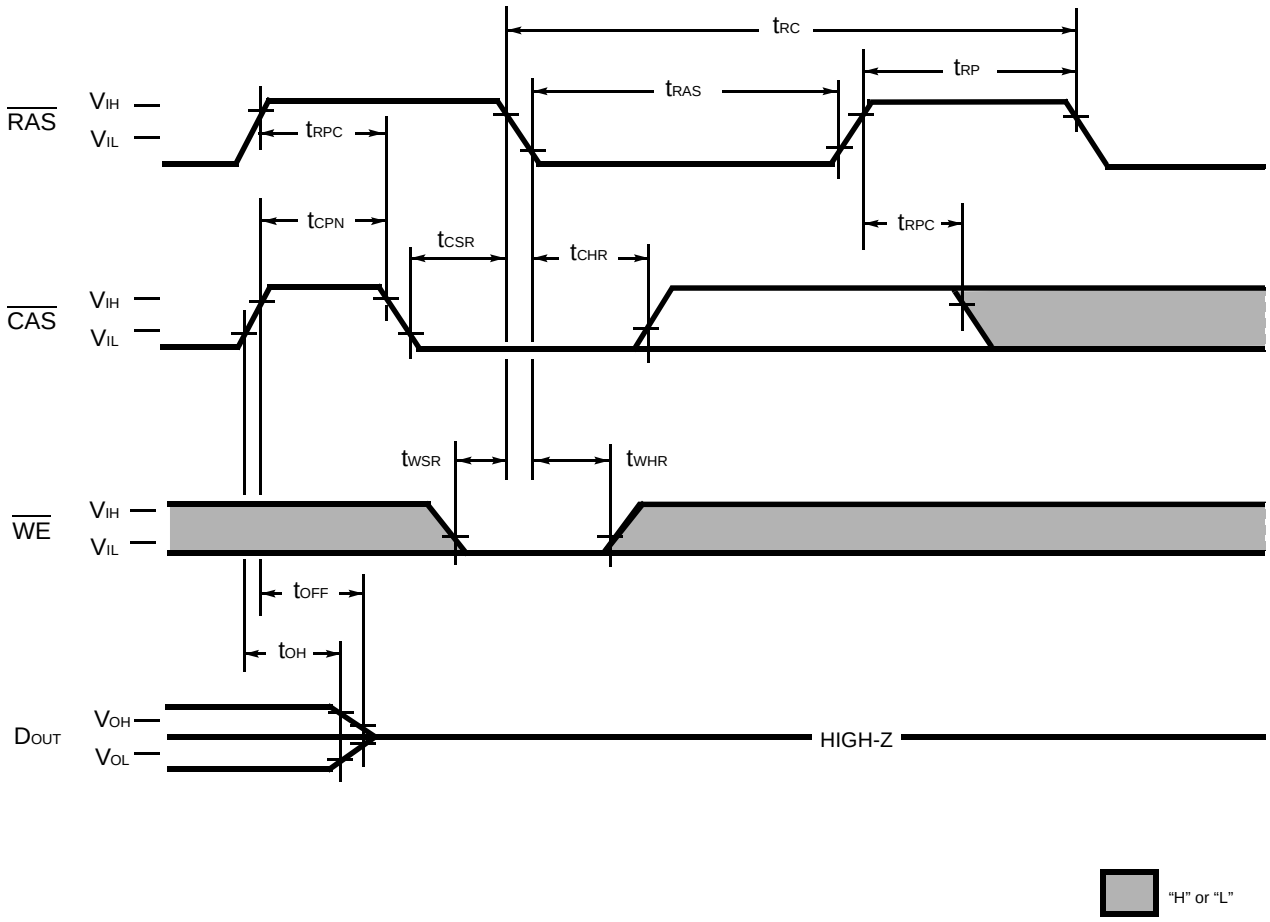
Fig.14 – TEST MODE SET CYCLE (A_O to A_{IO}, D = ”H” or ”L”)



DESCRIPTION

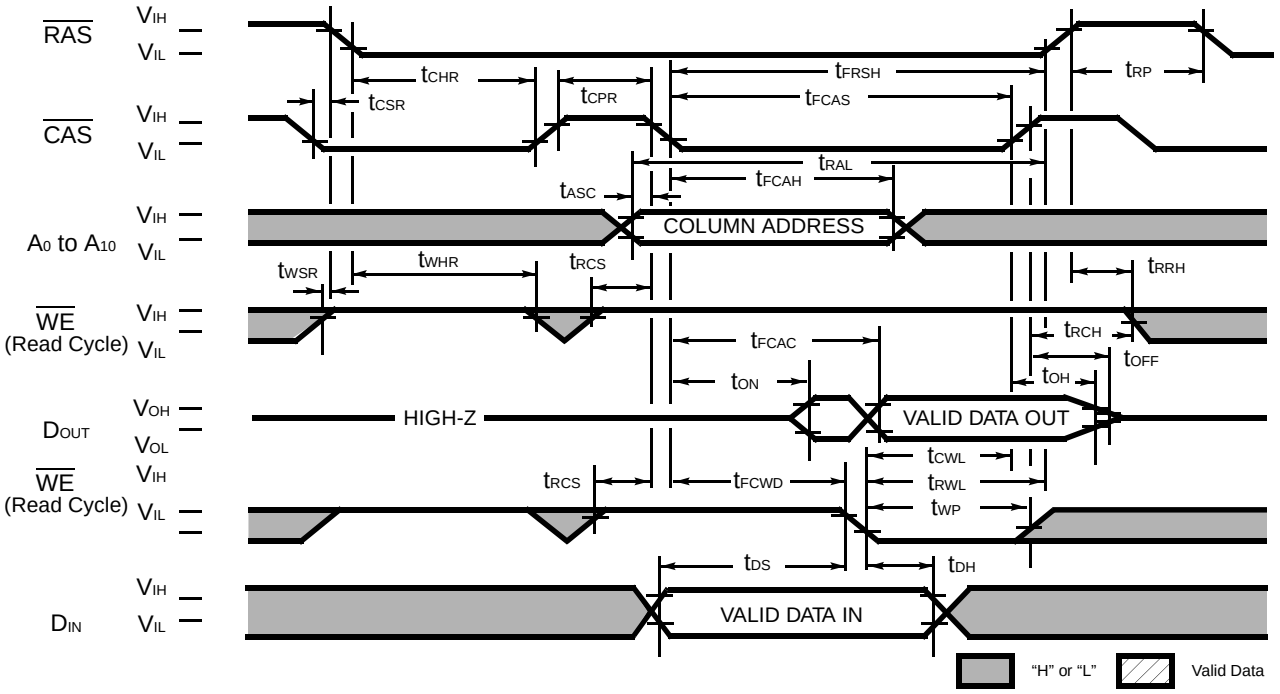
Test Mode ;

The purpose of this test mode is to reduce device test time to one eighth of that required to test the device conventionally. The test mode function is entered by performing a $\overline{WE}$ and $\overline{CAS}$-before-$\overline{RAS}$ (WCBR) refresh for the entry cycle.
In the test mode, read and write operations are executed in units of eight bits which are selected by the address combination of RA_{IO}, CA_O and CA_{IO}. In the write mode, data is written into eight cells simultaneously. In the read mode, the data of eight cells at the selected addresses are read back and checked in the following manner.

When the eight bits are all ”L” or all ”H”, a ”H” level is output.
When the eight bits show a combination of ”L” and ”H”, a ”L” level is output.

The test mode function is exited by performing a $\overline{RAS}$-only refresh or a $\overline{CAS}$-before-$\overline{RAS}$ refresh for the exit cycle.
In test mode operation, the following parameters are delayed approximately 5 ns from the specified value in the data sheet.
t_{RC}, t_{RWC}, t_{RAC}, t_{AA}, t_{RAS}, t_{CSH}, t_{RAL}, t_{RWD}, t_{AWD}, t_{PC}, t_{PRWC}, t_{CPA}, t_{RHCP} , t_{CPWD}, t_{RASP} , t_{RSH}, t_{CAS}, t_{CWD}, t_{CAC}.

Fig. 15 – $\overline{\text{CAS}}$-BEFORE–$\overline{\text{RAS}}$ REFRESH COUNTER TEST CYCLE



DESCRIPTION

A special timing sequence using the $\overline{\text{CAS}}$-before-$\overline{\text{RAS}}$ refresh counter test cycle provides a convenient method to verify the functionality of $\overline{\text{CAS}}$-before-$\overline{\text{RAS}}$ refresh circuitry. If, after a $\overline{\text{CAS}}$-before-$\overline{\text{RAS}}$ refresh cycle. $\overline{\text{CAS}}$ makes a transition from High to Low while $\overline{\text{RAS}}$ is held Low, read and write operations are enabled as shown above. Row and column addresses are defined as follows:

Row Address: Bits A_0 through A_9 are defined by the on-chip refresh counter.

Column Address: Bits A_0 through A_9 are defined by latching levels on A_0-A_9 at the second falling edge of $\overline{\text{CAS}}$.

The $\overline{\text{CAS}}$-before-$\overline{\text{RAS}}$ Counter Test procedure is as follows ;

1) Initialize the internal refresh address counter by using 8 $\overline{\text{RAS}}$ only refresh cycles.

2) Use the same column address throughout the test.

3) Write "0" to all 1024 row addresses at the same column address by using normal write cycles.

4) Read "0" written in procedure 3) and check; simultaneously write "1" to the same addresses by using $\overline{\text{CAS}}$-before-$\overline{\text{RAS}}$ refresh counter test (read-modify-write cycles). Repeat this procedure 1024 times with addresses generated by the internal refresh address counter.

5) Read and check data written in procedure 4) by using normal read cycle for all 1024 memory locations.

6) Reverse test data and repeat procedures 3), 4), and 5).

(At recommended operating conditions unless otherwise noted.)

No.	Parameter	Symbol	MB814100D-60		MB814100D-70		Unit
			Min.	Max.	Min.	Max.	
51	Access Time from $\overline{\text{CAS}}$	t_{FCAC}	—	15	—	20	ns
52	Column Address Hold	t_{FCAH}	15	—	15	—	ns
53	$\overline{\text{CAS}}$ to WE Delay	t_{FCWD}	15	—	20	—	ns
54	$\overline{\text{CAS}}$ Pulse Width	t_{FCAS}	15	—	20	—	ns
55	$\overline{\text{RAS}}$ Hold Time	t_{FRSH}	15	—	20	—	ns
56	$\overline{\text{CAS}}$ Precharge Time	t_{CPT}	30	—	35	—	ns

Assumes that $\overline{\text{CAS}}$-before-$\overline{\text{RAS}}$ refresh counter test cycle only.

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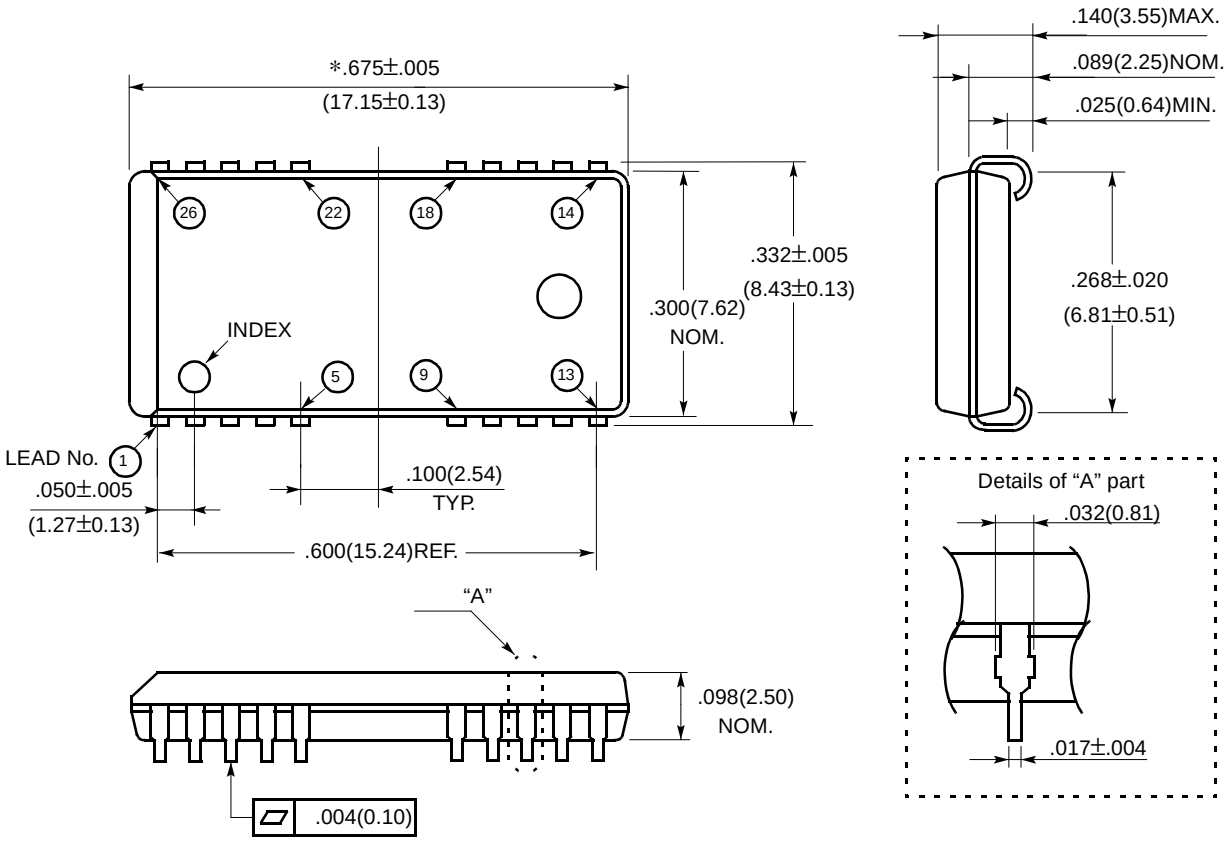
■ PACKAGE DIMENSIONS

26-LEAD PLASTIC LEADED CHIP CARRIER



*:Resin protrusion. (Each side:.006(0.15)MAX.)
Note: Although this package has 20 leads only, its pin positions are the same as that of 26-lead package.

Dimensions in inches (millimeters)

FUJITSU LIMITED

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